In the claims:

Please substitute the following full listing of claims for the claims as originally filed or most recently amended. Claims 1 - 9 have been canceled without prejudice or disclaimer.

1. - 9. (Cancelled)

10. (Previously Presented) A structure that adjusts carrier mobility in CMOS transistors comprising:

a substrate,

a first transistor having a gate dielectric, gate electrode, and source, drain, and gate regions, formed on said substrate,

a second transistor having a gate dielectric, gate electrode, and source, drain, and gate regions, formed on said substrate,

a first film providing tensile stress at least at the channel of said first transistor,

a second film providing compressive stress at least at the channel of said second transistor, a portion of said second film extending in the same region of said substrate as a portion of said first film, and

a shear force isolation layer separating said first film and said second film and said tensile and compressive stress therein in at least one area.

11. (Currently Amended) A structure as recited in claim 10, wherein said first film and said second film can be composed of nitride, oxide, or other material that exhibits either tensile or compressive properties, respectively, corresponding to said tensile stress in said channel of said first transistor or said compressive stress in said channel of said second transistor.

12. (Previously Presented) A structure as recited in claim 10, wherein said first film and said second film are separated by said shear force isolation layer at all points of overlap.

13. (Previously Presented) A structure as recited in claim 10, wherein said first film, is closer to the substrate than said second film, and does not fully surround said first transistor, but rather the sides only, while the remaining surfaces of said first transistor are contacted by said shear force isolation layer.

14. (Previously Presented) A structure as recited in claim 13, wherein said shear force isolation layer is the only separation between said first transistor and said second film.

15. (Previously Presented) A structure as recited in claim 13, wherein said shear force isolation layer surrounds the majority of an oxide liner of said second transistor gate electrode except the top of the gate which engages directly with said second film.

16. (Previously Presented) A structure as recited in claim 10, wherein said first film and said second film are separated by said shear force isolation layer at selected areas.

17. (Previously Presented) A structure as recited in claim 16, wherein said first film, closer to said substrate than said second film, fully surrounds said first transistor.

18. (Previously Presented) A structure as recited in claim 17, wherein said first film is the only separation between said first transistor and said second film.

19. (Previously Presented) A structure as recited in claim 17 wherein said second film surrounds said oxide liner at the sides of said second transistor gate electrode with the top of the gate directly engaged with said second film.